CLAIMS

1. An apparatus comprising:

an analog circuit configured to present a plurality of samples of an input signal in response to a plurality of phases of a reference clock;

a first digital circuit configured to generate (i) one or more data signal, (ii) a first strobe signal, and (iii) a second strobe signal in response to said plurality of samples, said plurality of phases, and a correction signal; and

a second digital circuit configured to generate said correction signal and a width signal in response to (i) said one or more data signal, (ii) said first strobe signal, and (iii) said second strobe signal.

2. The apparatus according to claim 1, wherein said second digital circuit is configured to store a number of width measurements for HIGH data symbols and a number of width measurements for LOW data symbols.

3. The apparatus according to claim 2, wherein said second digital circuit is configured to calculate an average bit

width in response to a comparison between (i) said stored widths of said number of HIGH data symbols and (ii) said stored symbol widths of said number of LOW data symbols.

4. The apparatus according to claim 3, wherein said second digital circuit is configured to compare (i) a measured width of a current HIGH symbol to the stored widths of previously measured HIGH symbols and (ii) a measured width a current LOW symbol to the stored widths of previously measured LOW symbols, wherein one or more parameter associated with said stored symbol widths is adjusted in response to said comparison.

5. The apparatus according to claim 4, wherein said first digital circuit is configured to adjust a current symbol width measurement in response to said correction signal.

6. The apparatus according to claim 2, wherein said second digital circuit is configured to store said width measurements in order of relative length.

7. The apparatus according to claim 2, wherein said second digital circuit is configured to (i) compare a current width measurement for a HIGH data symbol with stored width measurements for HIGH data and (ii) compare a current width measurement for a LOW data symbol with stored width measurements for LOW data.

8. The apparatus according to claim 7, wherein said second digital circuit is further configured to either store or discard said current width measurement in response to a result of said comparison.

9. The apparatus according to claim 1, wherein said second digital circuit is configured to generate said correction signal in response to a comparison between a number of stored HIGH width measurements and a number of stored LOW width measurements.

10. The apparatus according to claim 9, wherein said correction signal is generated in response to a comparison between each of said stored HIGH width measurements and a corresponding stored LOW width measurement.

11. The apparatus according to claim 2, wherein said second digital circuit is configured to store a predetermined score with each width measurement.

12. The apparatus according to claim 7, wherein a score associated with each stored width measurement is adjusted in response to said comparison.

13. The apparatus according to claim 12, wherein said score is incremented or decremented by a predetermined amount.

14. The apparatus according to claim 12, wherein said second digital circuit is configured to detect a locked condition in response to said score associated with each stored width measurement having a predetermined value.

15. An apparatus comprising:

means for generating a plurality of samples of an input signal in response to a plurality of phases of a reference clock;

means for generating (i) one or more data signal, (ii) a first strobe signal, and (iii) a second strobe signal in response

to said plurality of samples, said plurality of phases, and a correction signal; and

means for generating said correction signal and a width signal in response to (i) said one or more data signal, (ii) said first strobe signal, and (iii) said second strobe signal.

16. A method for determining a correct width of a bit of an input data stream comprising the steps of:

(A) determining a current data width and current data type of a symbol in said input data stream in response to said input data stream, a plurality of phases of a reference clock, and a correction signal; and

(B) generating said correction signal and a width signal in response to (i) said current data width and (ii) said current data type.

17. The method according to claim 16, wherein the step (B) comprises the sub-step of:

assigning a predetermined score to said current data width.

18. The method according to claim 17, wherein step (B) further comprises the sub-step of:

storing a number of data widths and associated scores based on an associated data type.

19. The method according to claim 18, wherein step (B) further comprises the sub-step of:

adjusting a score of one or more stored data widths either up or down based on said current data width.

20. The method according to claim 19, wherein step (B) further comprises the sub-step of:

repositioning said stored data widths and associated scores in a table based upon said current data width.